Dislocation-free Ge/Si coupling at LCM of their lattice constants, replacing InGaAs/InP

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Abstract **Currently, InGaAs-on-InP image sensors are used for SWIR imaging. The lattice constants of InGaAs and InP can be matched at 0.5869 nm by adjusting the ratio of In and Ga in InGaAs at 53 vs. 47. Ge and Si are much common materials than InGaAs and InP. However, Ge-on-Si image sensors generate much higher dark current than InGaAs/InP ones. The reason is the mismatch of the lattice constants of Ge, 0.5658 nm, and Si, 0.5431 nm, with a 4.18% difference, causing dislocations at the Ge boundary layer over the Si layer. The dislocations, especially threading dislocations which diagonally penetrate the Ge layer, generate huge dark current. This note provides a simple, yet, perfect solution to solve the problem. The concept is "A polka-dot coupling at pseudo LCM (least common multiple) of the lattice constants of Ge and Si crystals", in which the Ge and Si layers are connected through an array of openings of an insulation layer separating the Ge and Si layers with the pitch of a sort of LCM of the lattice constants of the Ge and Si crystals.**

***Key words*: Ge, image sensor, dislocation free, LCM Polka-dot coupling Introduction**

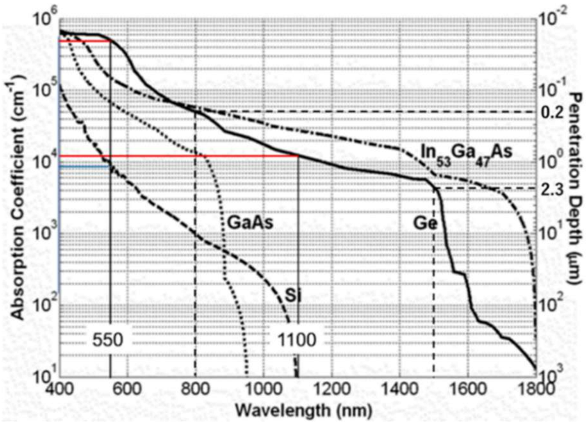

Fig. 1 Absorption coefficients and penetration depths vs. Wavelengths

I. Introduction

Currently, SWIR image sensors are using an InGaAs photo-electron conversion layer supported by an InP relaxation layer. Ge-on-Si has been a prospective combination of the materials for NIR and SWIR imaging with the effective wavelength up to 1500 nm (Fig. 1). However, difference of 4.18% of the lattice constants of Ge, 0.5658 nm, and Si, 0.5431 nm, generates dislocations (fine cracks) in the Ge layer over the Ge/Si interface with the height of 20 nm to 40 nm and the pitch of about 10 nm. On the other hand, the lattice constants of InGaAs and InP can be matched at 0.5869 nm by adjusting the ratio of In and Ga in InGaAs at 53 vs. 47.

This paper proposes a technology to break through the fundamental difficulty associated with direct coupling of a Ge crystal and a Si crystal. The technology is named "Polka-dot coupling at pseudo-LCM (least-common multiple) of the lattice constants of Ge and Si crystals". Fig. 2 conceptually explains the technology. Polka-dot is a fashion pattern which became popular in early 1800s with polka dance and music.

Assume that:

(1) the Ge and Si layers are separated by an insulation layer with an array of small openings filled with Ge and/or Si crystals along the direction of the lattice constants, and

(2) there are twenty four Ge atoms and twenty five Si atoms between adjacent openings.

Then, the length of a Ge atom chain between the openings is: 13.5792 nm (=24×0.5658 nm), and that of a Si atom chain is:

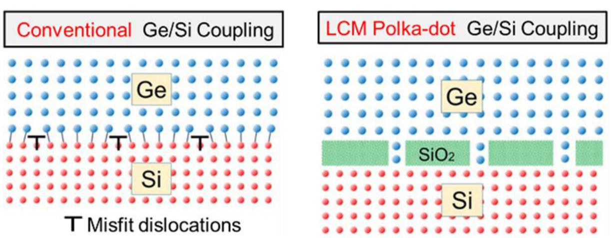

Fig. 2 Conceptional explanation of LCM polka-dot Ge/Si coupling

13.5775 nm (=25×0.5431 nm).

Upper four digits are effective. Therefore, if the pitch of the openings is 13.58 nm, there is no horizontal dislocation between a Ge atom above the opening and a Si atom below the opening.

Experimentally, the pitch of the dislocations at the Ge/Si interface without an insulation layer is about 10 nm, which is close to 13.58 nm. The pseudo-LCM theory seems to explain this empirical finding.

II. Conjugate Pitch of Openings

A. Ge/Si Conjugation with Openings on Insulator

Since 1990s, scientists have been struggling on zero-defect conjugation of Ge and Si crystals through an insulation layer with tiny openings.

Fig. 3 shows an example of a TEM image published by Li et al. in 2005 [1]. A SiO_2 layer of the thickness of several atoms on a Si layer are chemically roughened to expose at random the Si surface of several nanometers, and a Ge crystal are grown on the surface like a balloon. However, some crystal disturbances are observed around the opening. Worst of all, when adjacent balloons meet, the boundary becomes a crystal fault.

Nanohole array is one of the most exciting research topics. If the pitch is controlled to coincide with a common characteristic distance of the Ge and the Si crystals, the fault at the neighboring Ge-atom balloons will disappear.

B. Intrinsic Ge and Si Crystals

The pitch of 13.58 nm of the openings was not found accidentally. LCM is defined for natural numbers. The concept is borrowed for decimals. The pseudo-LCM is applied to the lattice constants of Ge and Si, which corresponds to the case with intrinsic Ge and Si atom chains along the [010] direction on the (001) plane. Assume that the numbers of atoms on a Ge atom chain and a Si atom chain are respectively N and (N+1), where N is a real number (not an integer). Then,

$$N\times 0.5658=(N+1)\times 0.5431. \qquad (1)$$

Then,

$$N=23.93, \text{ and } N\times 0.5658=13.54 \text{ nm}. \qquad (2)$$

The number of the Ge atoms, 23.93, is close to an integer, 24, used in the previous section, which was chosen for a realistic explanation.

C. Integer Pitch Openings

For the case presented in the introduction, the numbers of Ge atoms and Si atoms are integers. In practical applications for a very fine process, the pitch of the openings is expected to be an integer. The pitch can be an integer by adding a very small number of Si atoms to the Ge layer.

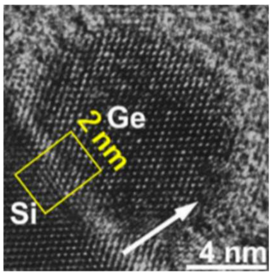

Fig. 3 A Ge balloon grown on an opening of SiO_2 layer [1].

Assume that the lattice constant of the Ge layer slightly shrinks to x from0.5658 nm with additional Si atoms to adjust the lattice constat to 14 nm. Then,

$$N\times x = (N+1)\times 0.5431=14. \qquad (3)$$

$$\text{Then, } x = 0.5650 \text{ nm, and } N = 24.78 \qquad (4)$$

Assume the lattice constant of a SiGe crystal be proportional to the portion of the Ge and Si atoms. Then, the portion of the Si atoms added to the Ge crystal is 3.5%.

However, N and (N+1) for the Ge and Si atom chains are 24.78 and 25.78, which are not integers. Therefore, the positions of the Ge and Si atoms deviate from the exact center of each opening by a half of the lattice constant at maximum.

In the case, one Si atom is added to a Ge atom chain with about thirty (≈1/0.035) Ge atoms.

III. Toward 1550 nm

A. Addition of Sn to Ge layer

In the previous case, the Si atoms additional to the Ge crystal slightly decreases the upper limit of the effective wavelength of the Ge layer from 1500 nm. A wavelength of 1550 nm is a magical one, since it is the most efficient optical window for observations through atmosphere and for optical communication through glass fibers.

There are some existing technologies to extend the upper limit of the effective wavelength of Ge crystal layers as follows:

(1) addition of a small number of Sn atoms to the Ge crystal,

(2) thermal stretch of the Ge crystal by using differences of thermal expansion coefficients of relating materials, and

(3) mechanical stretch of a very narrow Ge crystal bridge made with a micro-nano process.

The last one is out of focus of this note. The first and the second countermeasures are explained below.

Table 1 shows lattice constants, thermal expansion coefficients and melting points of typical materials used for image sensors with visible to SWIR light.

Fig. 4 shows a stack of a Ge and Si layers separated by an insulation layer with 5-nm openings at the pitch of 25 nm. There are forty-six Si atoms and forty-four Ge atoms

Table 1 Lattice constants, thermal expansion coefficients and melting points of typical materials used for image sensors with visible to SWIR light

	Atoms/ Molecules	Lattice constants (nm)	Thermal Expansion Coefficients ($\times 10^{-6}K^{-1}$)	Melting Points (℃)
Crystals	C	0.3567 (Diamond)	0.8	—
	Si	0.5431	2.556	1,414
	Ge	0.5658	5.79	938
	GaN	a.0.3186 c.0.5186	5.59	1,600
	InSb	0.6479	5.37	524
Insulators	SiO_2		0.55	1,710
	Al_2O_3		8.2	2,051
	HfO_2		6.0	2,758

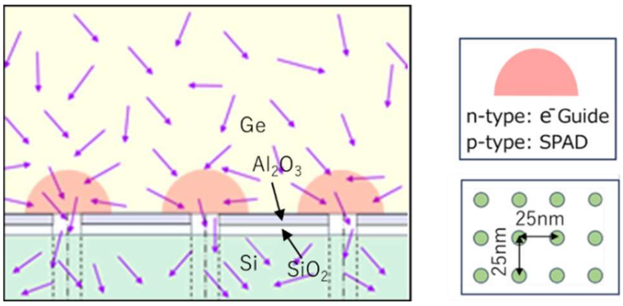

Fig. 4 Ge and Si layers separated by an insulation layer stack of Al_2O_3 and SiO_2

in an atom chain from an opening to an adjacent opening, where an atom at one of the edges of the atom chain is not counted.

Then, the length of the chain of the Ge atoms is:

$$24.90 \text{ nm } (=44 \times 0.5658 \text{ nm}). \quad (5)$$

The length of the Si atom chain is 46 × 0.5431 nm=24.98 nm. A very small ratio of Ge atoms can be added to make the Si atom chain exactly equal to 25 nm.

The lattice constant of Sn is 0.6493 nm [2]. The deficit of 0.10 nm from 25 nm can be compensated by replacing one Ge atom by one Sn atom from a Ge atom chain with thirty-seven Ge atoms. Then,

$$(36 \times 0.5658+0.6493)/37 \times 44=24.99\text{nm}. \quad (6)$$

When the ratio of the Sn atoms in the Ge crystals is below 8%, the Sn keeps the property as a semiconductor material. One Sn atom replacing one of thirty-seven Ge atoms satisfies the condition.

Some investigation is necessary to confirm if the upper limit of the effective wavelength exceeds 1550 nm by introduction of the Sn atoms or not. However, the technique can be combined with other technologies to extend the upper limit.

In this case, both the numbers of the Ge and Si atoms and the pitch of the openings are both nominally integers.

B. Utilization of Thermal Stress

For example, the thermal expansion coefficient of Si is about five-time larger than that of SiO_2 (2.556×10^{-6} K^{-1}/0.55×10^{-6} K^{-1}). The thermal expansion coefficient of Ge is about ten-time larger than that of SiO_2 (=5.79×10^{-6} K^{-1}/0.55×10^{-6} K^{-1}). Therefore, when a Si or Ge layer grows on a SiO_2 layer at several hundred degrees C, and is cooled to a room temperature, a strong tension works on the Si or Ge layer, extending the upper limit of the effective wavelength.

However, the stacking of the Ge layer over the SiO_2 layer requires a careful observation in the process to avoid possible generation of fine cracks in the Ge layers.

A stack of an Al_2O_3 layer over a SiO_2 layer mitigates the tension between the Ge layer and the insulation layer, since the thermal expansion coefficient of Al_2O_3 is 8.2×10^{-6} K^{-1}, which is about 1.2 times that of Ge.

Usually, a negative fixed charge associated with the Al_2O_3 layer is used to suppress signal electrons approaching the defective interface between the SiO_2 insulation layer and the Si or Ge crystal layer.

Melting points are also important in the process. For example, stacking of Si, Ge and InSb is eased by taking their melting points into consideration. Their melting points are 1,414 degrees C for Si, 938 degrees C for Ge, and 524 degree C for InSb. Though their process temperatures are much lower than the melting points, they are fundamentally dependent on the order of the melting points. In fact, Si is processed in a wide temperature range around 900 degrees C, and Ge around 500 degrees C.

IV. Process Issues

A. 5-nm Diameter of Openings

For the pitch of the openings of 10 nm to 30 nm, which appeared in the previous sections, the diameter of the openings is hopefully less than 5 nm. Well-controlled manufacturing of solid-state nanopore arrays is one of exciting research topics [3]. One of promising technologies to make such a small openings is EBL (Electron-beam Lithography). The beam diameter is currently less than 5 nm. However, it is still difficult to make 10-nm openings even with EBL.

In fundamental research, it is possible to make the diameter even less than 1 nm by means of ALD (Atomic Layer Deposition) of SiO_2, Al_2O_3 or HfO_2 [4,5]. The Al_2O_3 layer accumulates over the vertical walls of the openings as well as the flat surface of the insulation layer. One problem is the accumulation of Al_2O_3 at the bottom of the openings which insulates the Ge layer from the Si layer. Then, dry etching can remove the Al_2O_3 at the bottom, keeping the Al_2O_3 layers over the walls. Even, when the walls are inclined, only the oxide layer remains after dry etching as shown in the next section.

It will take at least five years before the proposed technology is going to be applied to a practical image sensor process. The current most advanced fine process is at the 3-nm node. For this process, the minimum wiring pitch (wire width+space) is 45 nm, and the wire width is 20 nm. It will take more than five years to reach 12 nm,

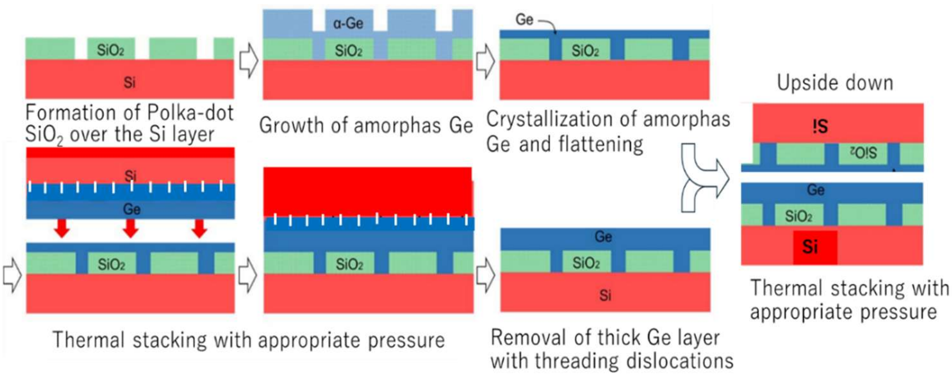

Fig. 5 Fabrication of a Si/Insulator/Ge/Insulator/ Si stack (Practically, the insulator is made with a stack of Al_2O_3 and SiO_2 layers)

since the light source is EUV (Extreme Ultra Violet) light of which wavelength is 13.5 nm. Research to further reduce the process is going on to achieve 6 nm wiring by means of FEL (Free-Electron Laser).

B. Imaging from Visible to SWIR Light

S. Manda, et. al. developed an image sensor with a wide optical window from visible to SWIR light with a InP/InGaAs/InP stack [6]. Theoretically, a Si/Ge/Si stack separated by SiO_2 with openings can be fabricated. However, it is difficult to generate the SiO_2 and Si layers on the Ge layer. The reasons are:

(1) the process temperatures of SiO_2 and Si are much higher than that for the Ge layer, and

(2) GeO_2 is unstable, absorbing H_2O to be deteriorated.

Therefore, we will propose a process to combine an inverted Ge/SiO_2/Si layer, i.e., Si/SiO_2/Ge layer, onto another Ge/SiO_2/Si layer at several hundred-degree C as shown in Fig. 5. The experiment is now going on.

V. Threading-Dislocation-Free

A. 0.5-um Ge Photosensor

In the following sections, dislocations are allowed, but with no threading dislocations. A frequency of threading dislocations may nonlinearly decreases against a decrease of the size of the photosensor under a threshold size. For example, in advanced processes, the frequency of threading dislocations is less than 1 for the size of a Ge layer of less than 1 um.

Assume a macro-pixel is composed of 2×2 element pixels each with the photodiode of a 0.5-um square. An element pixel with threading dislocations generates an extraordinarily larger signal than a threshold value. An image signal of a macro pixel is calculated as an average of intensities of the image signals of the element pixels after neglecting ones generating exceptionally large image signals due to the threading dislocations. Then, if all four element pixels are suffered from exceptionally large image signals, no output is provided form the macro pixel. However, the probability is very low.

For example, when a occurrence probability of the threading dislocations is 1/2 per a 1-um square, the probability of the element pixel with threading dislocations is 1/8. Then, the probability that all four element pixels have threading dislocations is 0.000244 (=$1/8^4$). The signal of these macro pixels with no signals can be interpolated with those of surrounding macro pixels. On the other hand, 99.97 % of the macro-pixels provide their image signals.

Then, the resolution of the macro-pixel array is more than 50% of the resolution of the element pixel array. For example, the resolution of the images of 1024 × 1024 element pixels is higher than that of 512×512 macro-pixels. The sacrifice of the spatial resolution may be compensated by that there is practically no image suffered from the threading dislocations.

B. Inverted Pyramid Ge Photodiode

A pixel with a photodiode of a 0.5-um square can practically eliminate pixels with threading dislocations. However, a diffraction limit is about a half of the wavelength of the incident light. For SWIR light, it is 750 nm (=1500 nm/2) > 0.5 um. The diffraction limit covers about a half of the diameter of the Airy's dome. Therefore, to fully utilize the incident light, the diameter of the aperture is hopefully equal to or wider than the target wavelength.

We proposed an inverted pyramid photodiode as shown in Fig. 5 as the countermeasure. The four sides of the inverted pyramid are covered with a SiO_2 insulation layer and the bottom with a 0.5-um square is directly connected to a Si layer. The surface is wider than 2.5 um. We are developing a technology to create such a Ge inverted pyramid [7].

(1) At first, a surface of (100) Si is etched with a 20 wt% TMAH solution, A square pattern on the mask results in inverted pyramid structures with the depth of 500 nm,

(2) an oxide film is thermally grown all over the Si surfaces, and, then,

(3) etched by using RIE at the appropriate time, fully thickness of the slope surfaces.

Thinning of the bottom progresses earlier than the slope, and, finally, the Si layer at the bottom is fully disclosed with a thin SiO_2 layer on the slope remaining. Now, Ge atoms fill the inverted pyramid opening.

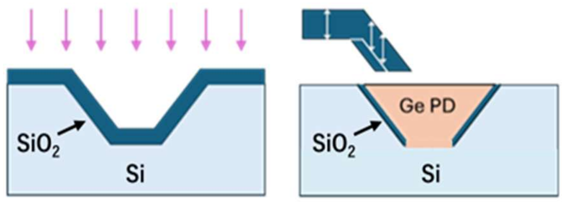

Fig. 5 Formation of a Ge pyramid (A selective etching rates to slopes and the bottom connects the Ge pyramid PD to the Si substrate, keeping thin insulation oxide side slopes)

References

[1] Q. Li, et al, Morphological evaluation and strain relaxation of Ge island grown on chemically oxidized Si (100) by molecular-beam epitaxy, *J. of Appl. Phys*., 98(7), 073504-8, 2005.

[2] M. Ishimaru, et al., Behavior of Sn in crystallization of GeSn, *Materia*, 59(12), 662-668, 2020.

[3] H. Liu, et al. Solid-State Nanopore Array: Manufacturing and Applications, *Small*, 19, 2205680, 1-29, 2023.

[4] P. Chen, T. Mitsui, et al., Atomic layer deposition to fine-tune the surface properties and diameters of fabricated nanopores, *Nano Lett*, 4(7), 1333-1337, June 25, 2004.

[5] TiO2, SiO2 and Al2O3 coated nanopores and nanotubes produced by ALD in etched ion-track membranes for transport measurements, *Nanotechnology*, 26, 335301, 2016.

[6] S. Manda et al, "High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer", *IEDM 2019*, 390, 2019.

[7] S. Oshima, T. Ando, et al., Fabrication of Ge-in-Si pyramid charge collection structures for high-speed imaging, *The 41th Sensor Symposium*, 25P2-C3, 2024.